CM6212+CM9881 USB Hi-Speed Audio

Layout Guide and Application Notes

Introduction

This document provides guideline for the design of USB 2.0 high-speed audio CM6212 for use with HAD codec CM9881 in boards. There are a multitude of methods for successful layout of high performance digital audio circuits. The material includes general various types of device implement, component placement considerations, trace routing considerations. For more detail please refer to engineer of the C-Media electronics corporation.

General Rule

1. If it's necessary to turn 90°, it's better to use two 45° turn or an arc, instead of making a single 90° turn as Figure 1. It can reduce reflection on the signal by minimizing impedance discontinuities.

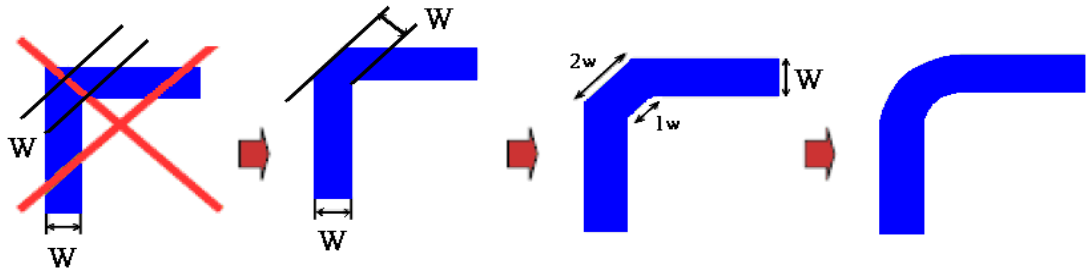

Fig.1 Turn Angle

2. Differential signal pair impedance control and connector. The USB 2.0 D+/D- differential pair, which can operate at a rate of 480MBPS (High-Speed), are some of the most critical signals on a PCB. Its implementation on the PCB requires special considerations. The inductive and capacitive reactance, resistance, and conductance of a PCB differential pair will determine the impedance of the trace pair at any point along the PCB track. The value of differential impedance will be a function of the physical dimensions of the trace, as detail below. For a USB 2.0 differential pair, an impedance of 90Ω¸ is optimal.
3. For a USB board, the best image plane is the ground plane. Use of image planes provides low impedance, shortest possible return path for RF currents.

4. The old rules of splitting power and ground into “digital” and “analog” sections do necessarily apply to the many audio devices. AGND and APWR plane as the same region as possible, place DGND and DPWR plane on other region.
5. Use f-bead to connect different ground plane for the EMI issue.
6. Be tied together power plane at one point through a low-impedance bridge or preferably through a ferrite bead as Figure 2.

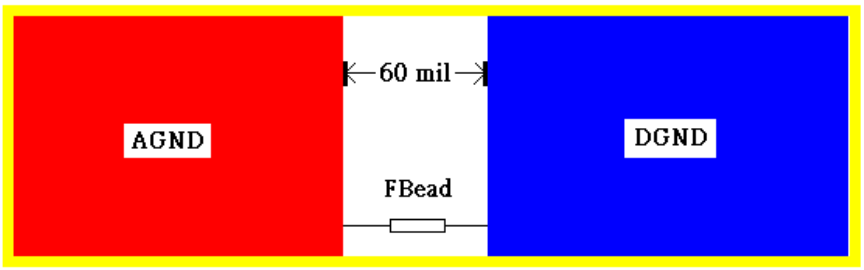

Fig.2 AGND and DGND

7. Place power bypass capacitors near OP-Amplifier, for more clean power.
8. Consider achieving proper ESD/EMI performance; use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the USB connector pin. If voltage regulators are used, place a 0.1μF capacitor on both input and output as Figure 3. This is to increase the immunity to ESD and reduce EMI.

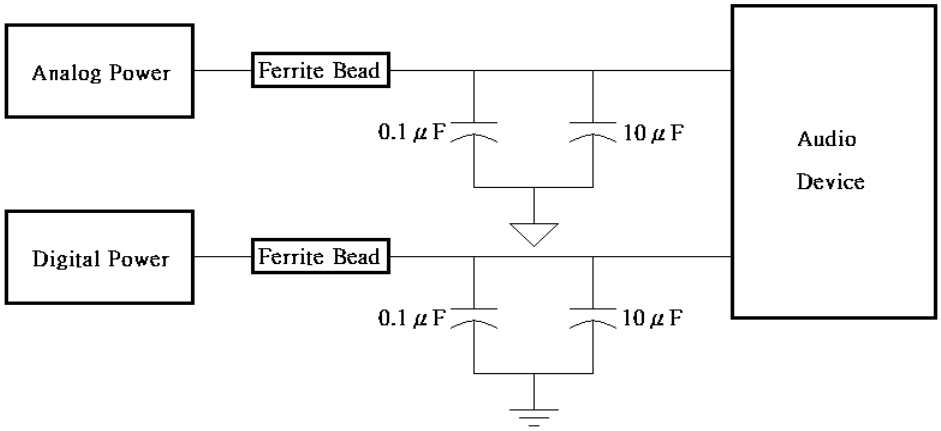

Fig.3 Capacitors Array

9. Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

USB 2.0 Trace Spacing

The physical construction of differential PCB traces as Figure 4, determines the differential impedance. The primary physical characteristics are summarized as following.

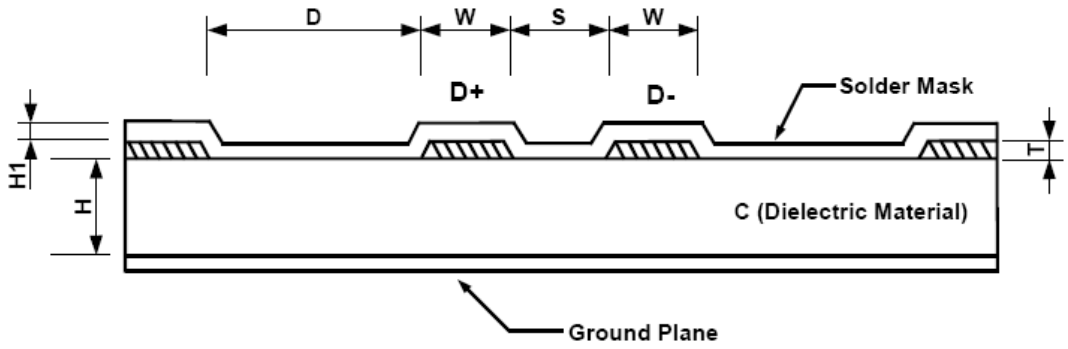

Fig.4 PCB stack up configuration (partial)

1. W = Width of the trace
2. S = Separation from D+ to D-
3. H = Dielectric thickness, distance of trace from the ground plane.
4. T = Thickness of the trace
5. D = Ground Separation
6. H1 = Solder mask thickness
7. Er = Dielectric constant (depend on C, example: FR4 Er =4.6)

The PCB designer should use an impedance calculator to determine the differential trace impedance of USB 2.0 differential signal pair. Note that the calculations to determine the differential impedance are somewhat different from those used to calculate the impedance of a signal trance.

The specific printed circuit board stack up is as follows table

W =20 mils	T = 1ounce
S =30 mils	Er ≈ 4.6 (FR4 material)
D ≥ 30 mils	Board thickness ≈ 63 mils (1.6 mm)
H ≈ 9 mils	Impedance ≈ 45Ω

In USB 2.0 applications, a PCB with a minimum of 4 layers is required. Because it needs to control the impedance of the USB 2.0 differential signal pair and supply a clear power and ground.

Layer Description Signification Features

The 4 layers are typically configured as described as below.

1. Component Side (Top)

   Contain differential signal pair and other signal routing and primary surface-mounted components.

2. Ground Layer

   Ground plane (include AGND and DGND), also is reference layer for differential signal pair.

3. Power layer

   Power plane (include AVCC and DVCC).

4. Solder Side (Bottom)

   Contains signal routing and secondary surface-mounted components.

Layer	Description	Signification Features
1	Component Side (Top)	Contains differential signal pair and other signal routing and main components.
2	Ground Layer	Ground plane (include AGND and DGND).
3	Power Layer	Power plane (include AVDD and DVDD).
4	Bottom Side	Contains signal routing and other components.

5. Because of the high frequencies associated with the USB, PCB with at least four layers is recommended; two signal layers separated by a ground and power layer.

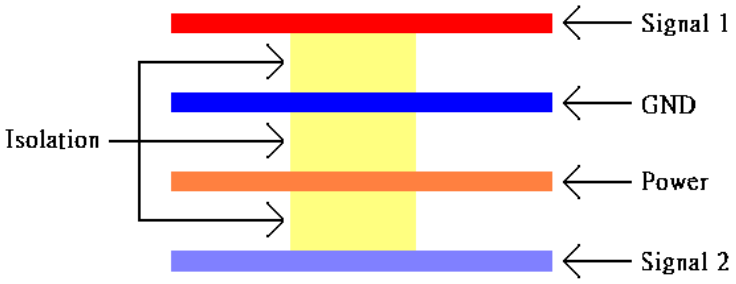

Fig.5 Four Layer Board

The majority of signal traces should run on a single layer, preferably signal1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

6. For a layout that helps to reduce noise, separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their respective ground planes. Placing analog power coincident with analog ground, and digital power coincident with digital ground (as Figure.6 – Recommended separation). If any portions of analog and digital plane overlap, the distributed capacitance (result from power plane reference to ground plane or signal plane reference to ground plane) between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolated plane (as Figure.6 – wrong separation). The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

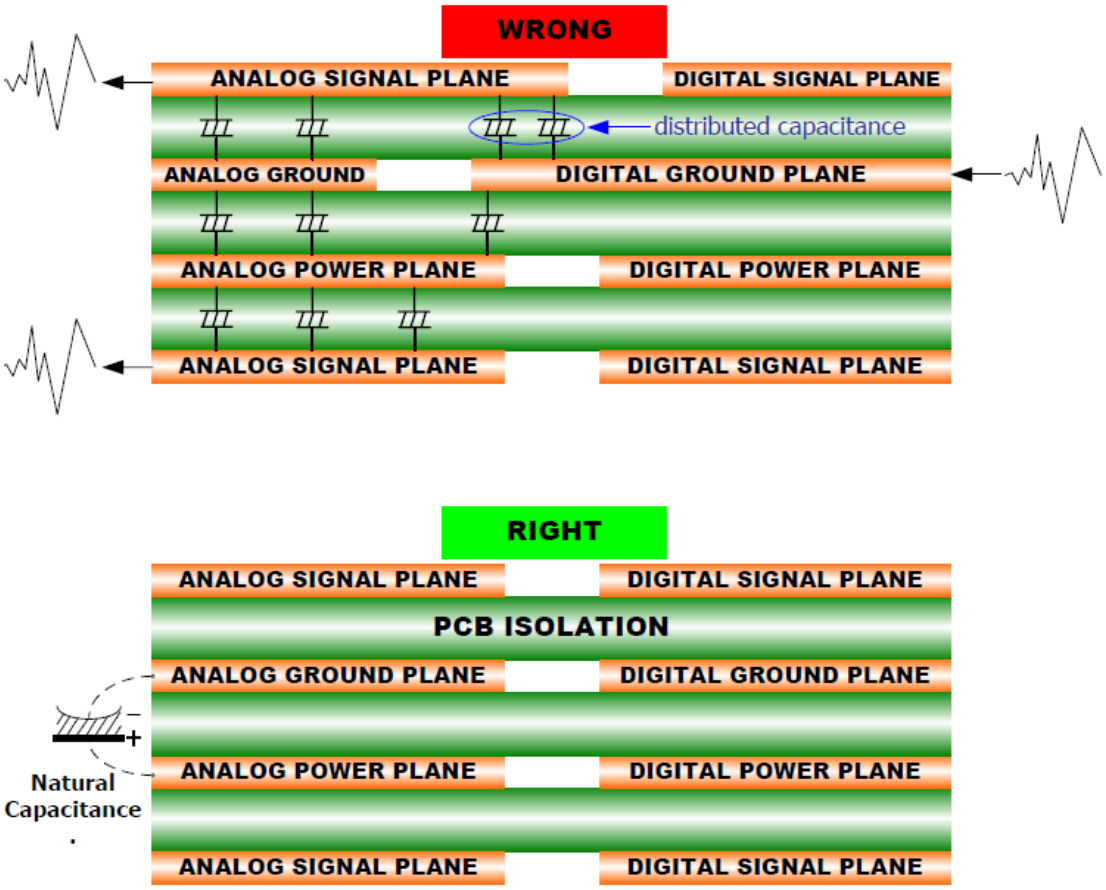

Fig.6 Cross section of PCB, the recommended separation for analog and digital plane.

Placement and Routing

1. Place the USB connector and the CM6212 audio chip on the un-routed board first, with minimum trace lengths, as equal as possible (D+, D-), route high-speed differential signal pair first. Keep appropriate distance between high-speed signals to USB 2.0 differential signal pair.
3. Route the USB 2.0 differential signal pair on the component side, which is adjacent to the ground plane layer. Vias to different signal trace layers or routing to close to breaks in the ground plane will adversely affect the differential trace impedance.
4. Route USB 2.0 differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change.
5. Please don't route USB 2.0 differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference.
6. Stubs on USB 2.0 differential signal pair should be avoided. While stubs exist, it will cause signal reflection and affect signal quality.
7. Route USB 2.0 differential signal pair traces over continuous ground and power planes. Avoid differential signal pair crossing anti-etch areas or any break in the underlying planes and routing the near the edge of the PCB or power planes.
8. Keep parallelism between D + and D-with the trace spacing, which achieves 90Ω differential impedance.
9. Route paths of SPDIF IN and OUT to separate t least 20 mils gap.
10. Do not allow any digital or analog signal traces pass through the drawbridge, otherwise, the digital noise may induced into the analog signals, makes audio performance worse.
11. Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through screw holes.
12. C-Media recommended to layout the width of each signal traces at least 10 mils and the space is the least one time the size of width of signal trace.
13. For ADC and DAC, VREF is also bypassed. Depending upon the converter architecture, the range of the large capacitor may be from 1uF to 47uF. Place bypass capacitor near chip.
14. Placement of the capacitor near the chips is very important. The bypass capacitors provide high speed current for the modulator operation, so the bypass capacitors are actually used to store charge for this high speed current draw.

Crystal selection

In crystal-based oscillator circuit, the oscillatory frequency is based almost entirely on the characteristics of the crystal in use. Therefore, it is important to select a crystal that meets the design requirements. It is strongly recommended to choose the crystal or oscillator with the absolute influence to the quality of transmitter signal and receiver signal. The feedback resistor R has been used on the PCB. It is necessary to add feedback resistor (1Mohms) on external circuit.

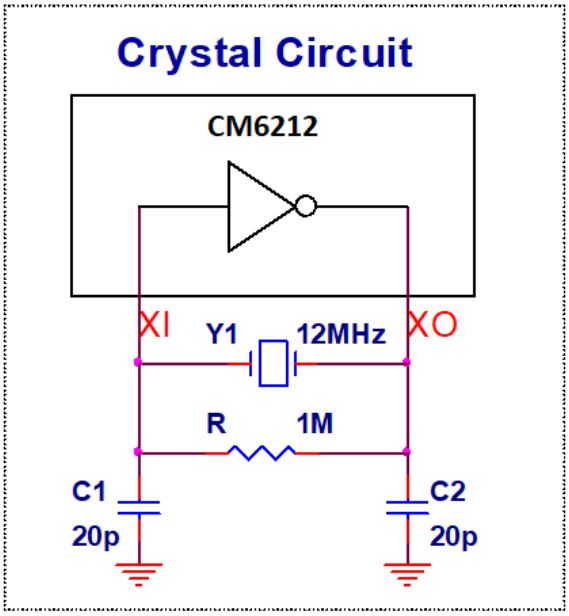

Fig.7 Crystal Circuit

Parameter	Typical Value
Nominal Frequency	12.000000MHz
Oscillation Mode	Fundamental
Frequency Tolerance	±30ppm
Load Capacitance	20pF
Shunt Capacitance	4~6pF(max7pF)
Effective Series Resistance	60ohms
Drive Level	100uW
Stability Over Temperature Range	30ppm
Operation Temperature Range	-10℃ ~ +70 ℃
Aging	±5ppm / year

The frequency tolerance shall be less than 30ppm. Load capacitance is a critical crystal parameter, which specifies the capacitive load that must be placed across the crystal pins to oscillate at the specified frequency. It influences the actual oscillation frequency, as the crystal manufacturer actually 'trims' the crystal to oscillate at its nominal frequency for t he specified load capacitance.

Passive Component Selection

Selection of passive components can have a profound effect on both sound quality and specification realization. Care must be taken to match the types of passive components with the end product objective.

Bypass Capacitor

1. The basic definition of a bypass capacitor is that it is used to conduct AC components in the power supply line around the data converter circuit. This AC component is removed from the DC supply, enabling the converter to achieve its stated performance specification. Failure to adequately remove AC noise from the power supply line will allow the noise to couple into the converter, resulting is dynamic performance reduction.
2. Power supplies require that at least two capacitors for bypassing: a large capacitor (nominally >10uF) for low frequencies noise and a small capacitor (nominally =0.1uF) for high frequencies noise. The actual value of the capacitors depends upon the noise characteristics of the power supply. If the noise is low frequency, increase the value of the large capacitor. If the noise is high frequency, add an additional capacitor with a smaller value than the previously selected small capacitor.

Capacitors

1. For power supply bypass capacitors and DC-blocking, we recommend using aluminum electrolytic. These capacitors open when they fail, which will prevent catastrophic system failures. However, at low temperature, some low-grade electrolytic capacitors degrade in capacitance, resulting in high distortion.Tantalum capacitors should be avoided for bypassing, since they short when they fail.
2. For filter capacitors that are in line with the audio signals, polypropylene film capacitors provide the best THD performance. For filter capacitors, be cautious of ceramics, which can induce piezoelectric effects into the system. This results in the board acting as a microphone for mechanical disturbances and vibrations.
3. The types commonly available in chip form are ceramic and electrolytic. Ceramic dielectric is more widely used because it is non-polarized, more stable over temperature,

and has lower “ESR” than either tantalum or aluminum electrolytic dielectric. Ceramic chip capacitors are recommended for these reasons.

4. CM9881 having AVDD=5V ±5%, so the capacitors must have a 10V working voltage. A working voltage of 16V is recommended to provide margin for variations in the application.All capacitors have a temperature coefficient (TC). This factor will affect system performance and must be taken into account. Low TC capacitors are preferred but may add cost.

Resistors

There are two types of resistors to consider: carbon and metal film. Each type has its advantages, depending on the primary objectives for the system performance. If sound quality is the top objective, we recommend using carbon film resistors. To maximize performance specifications (SNR and THD), you should use metal film resistors.

Coupling Capacitor

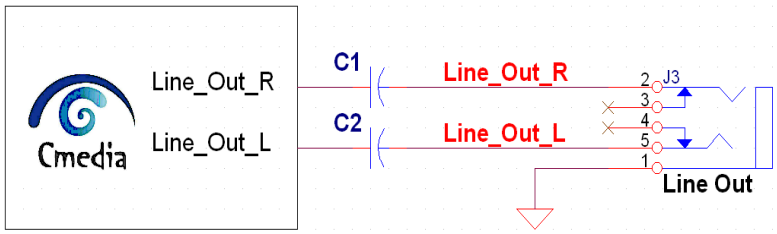

Fig.8 Coupling Capacitor

C1 and C2 are coupling capacitors. The purposes of capacitors are to isolate DC and pass AC. The coupling capacitors must have low inductance and low equivalent series resistance (ESR). All analog input/output path width must have up 20mils and separated AGND.

Analog audio input/output path

The width of IN/OUT signal traces are the least 10 mils and space is the least one time the size of width of the signal (According to the 3W rule, the best width of spacing is 3 times of width of the signal). shortest connection to pin with WIDE traces to reduce impedance.

CM9881 Capacitor design & Selection

1. Mount two reference capacitors as close as possible to the CM9881. This will optimize the PCB trace parasitic elements of series resistance, series inductance and parallel capacitance. All of these elements will affect JD-sense function. The series resistance of the PCB trace will look the same as capacitor ESR to the circuit and reduce the JD-sense noise.

   Reference capacitor values are critical. Since they are a component of the JD-sense circuitry, their value will affect its JD-sense function. So 10uF/X5R is recommended.

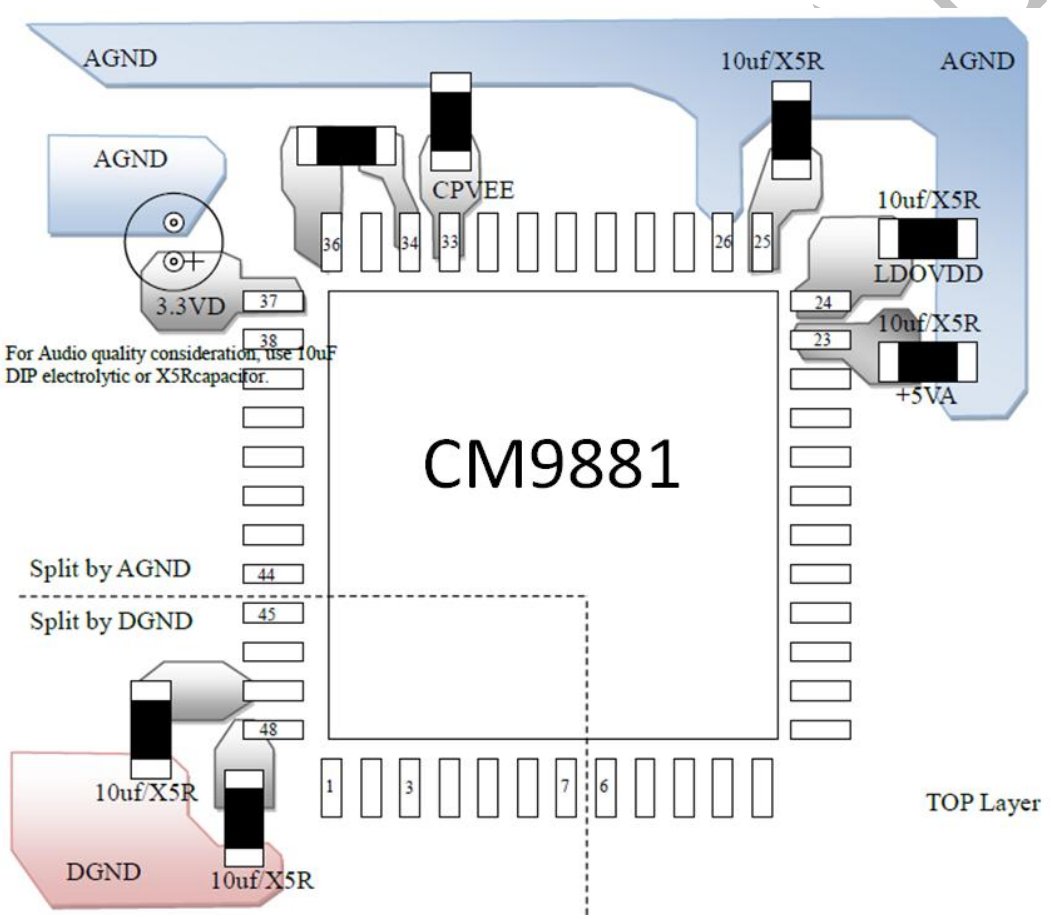

Fig.9 CM9881 Capacitor design

2. **Decoupling and bypassing capacitors**

   Bypass capacitors on the PCB are used to short digital noise into ground. Commonly, codec may generate noise when its internal digital circuitry is operating. The current changes arise in the power and ground pins for the related section of the codec. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through

the bypass cap and back into the codec through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the codec and the bypass capacitors when in the operating frequency of the codec. The longer the trace – the greater the inductance. To avoid long-trace inductance effects, use the shortest possible traces for bypass capacitors, with wide traces to reduce impedance. For best performance, use supply bypass leads of less than one-half inch.

Pins with a first – "A" priority components placed around the codec are the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10μF surface mount devices are good if they are used in conjunction with 0.1μF ceramics. The filter capacitors with "B" priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to codec. A good reference voltage is relative to good analog performance. These decoupling capacitors ("C" priority) should be close to the codec pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance. The Table I also point out the distribution of codec capacitor locations and placement priorities.

Signal Description	Priority of Close Proximity to Codec
Digital Supply Voltage , +5DVdd	A
Analog Supply Voltage, +5AVdd	A
Voltage Reference Filter(V_{REF})	B
Voltage Reference out (V_{REF_OUT})	B
Analog Signal Inputs(Decouple)	C

Capacitor placement priorities

3. The Anti-Glitch Capacitors

In practical situation, it is possible that there are glitches induced on LINK signals. Glitch on RESET- generated by chipset makes a misunderstanding to reset codec in run time. Glitch on SYNC makes codec loss synchronization with chipset, analog output will be corrupted. BCLK generated by controller sometimes has ring-back or overshoot phenomenon due to impedance mismatch at receive terminal, it may cause unstable LINK operation. Figure 10 suggests system designer reserve some anti-glitch capacitors at LINK bus, Ce10 and Ce11 used to anti-glitch on SYNC and RESET-. The ring-back resister Re6 and Ce6 are used to suppress overshoot and control slew rate on BCLK.

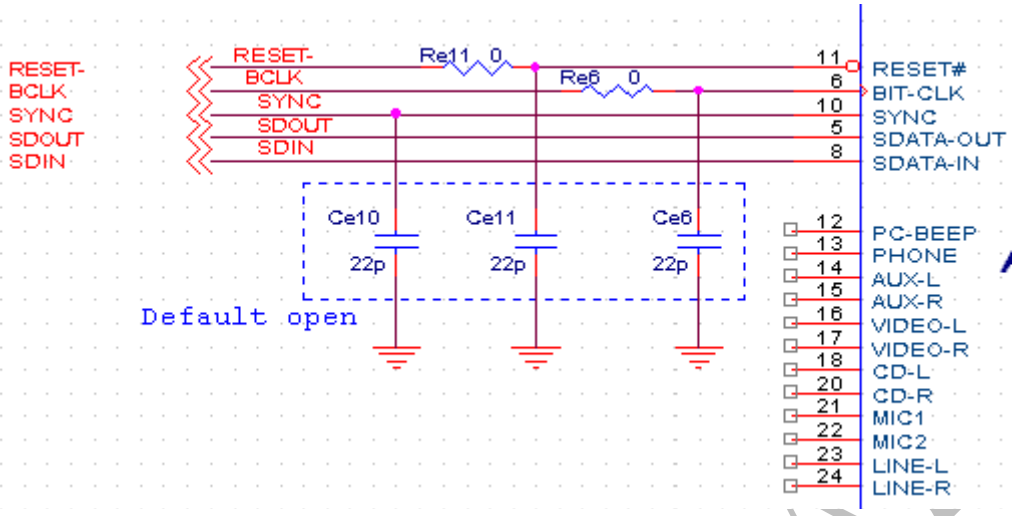

Figure 10. Reserved anti-glitch capacitors on LINK bus

4. Impedance

The LINK signals trace distance of the ground (dielectric thickness) , impedance are 55 Ω~60 Ω (± 15%).

Guard ring on PCB-edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. The field lines of the signal return to PCB ground as long as an “infinite” ground is available. Traces near the PCB-edges do not have this “infinite” ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable - should be accompanied by a guard ring on the PCB edge.

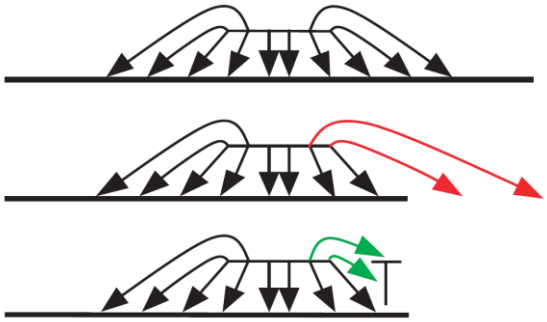

Fig.11 the field lines of the signal return to PCB ground

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 11. As these traces should have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Advantages of power planes

1. Easy and fast to implement
2. Low inductive power supply
3. Creates a capacity together with ground plane

Advantages of routed power supplies

1. Allows the usage of one layer for more than one supply system, thereby reducing the cross -talk between these supplies
2. May reduce cross-talk within each supply system
3. Requires more careful power routing
4. Higher supply impedance may require extra capacity for supply stabilization.

The optimum obviously is to apply the advantages of both methods. Therefore several local power planes should be implemented and connected to the supply via traces. Planes of different supply systems should be located in the same layer or separated by a ground plane to minimize crosstalk between these systems. Although the local power planes are easy to implement special care must be taken when connecting the power pins and the decoupling capacities to the planes.

(a) Connection of decoupling capacities

The decoupling of the most critical power supply pins of the microcontroller very often is the most fastidious part in a PCB design. Even in a multilayer design every millimeter of trace has to be carefully considered.

(b) Sketch equivalent circuits

When considering the best placement, direction and connection of the capacity a small sketch may be very useful. Each piece of wire shall be drawn as impedance even though the actual value is not important. The Figure 12 clearly indicates that the 2 red impedances should be minimized while the other 2 may be object to concessions.

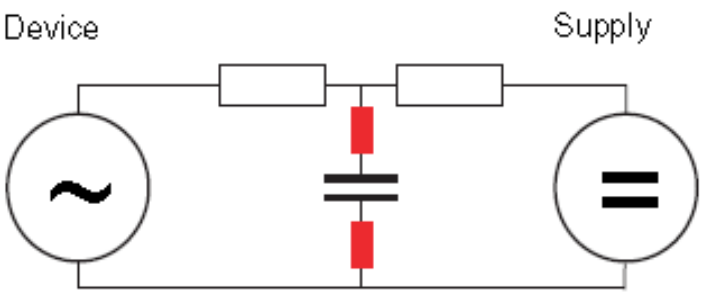

Fig.12

Cross Talk

A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 parts of next Figure indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.

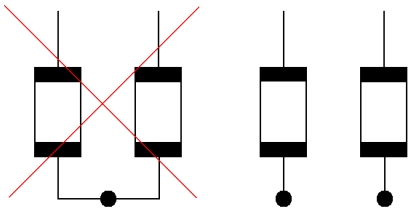

Fig.13 Bad Screw hole to Cross Talk

S/PDIF IO Layout Guide

1. Crosstalk is an undesirable feature with S/PDIF signals. It causes a disturbance between S/PDIF-IN and S/PDIF-OUT signals. Mutual coupling mechanisms will be form if S/PDIF-IN and S/PDIF-OUT are parallel, the mutual capacitance and mutual inductance between traces have capacitive and inductive coupling of electromagnetic field generated by S/PDIF-OUT. Figure 14, indicates the coupling energy from S/PDIF-OUT may interfere S/PDIF-IN operation.

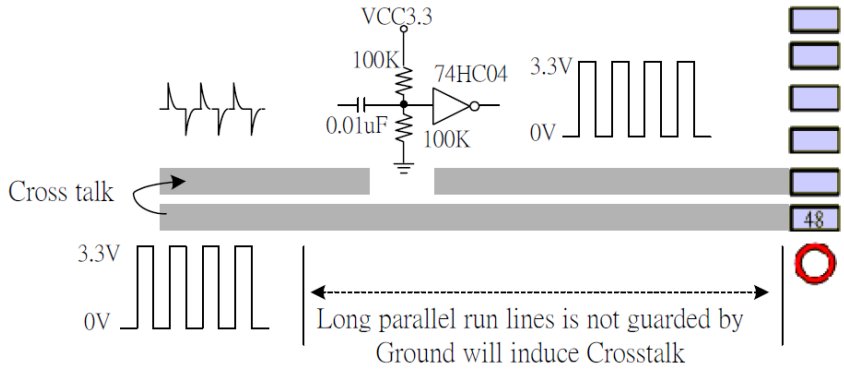

Figure.14 Crosstalk between S/PDIF-IN and S/PDIF-OUT traces

2. Design and layout rules listed here are useful to prevent crosstalk.
   A. Minimize physical distance between IO connector (or header) and CODEC.
   B. Avoid routing of S/PDIF-IN trace parallel to S/PDIF-OUT. equation to minimize crosstalk, distance (H) with reference plane must be minimized, and distance (D) between traces must be maximized.
   C. S/PDIF-IN and S/PDIF-OUT signals are separated by ground traces will reduce crosstalk.

D. A simple rule to minimize coupling between traces is the 3-W rule. The distance separation between centerline of traces must be three times the width of a single trace.

3. Additional to above layout rules, the 3-W rule represents the approximate only 70% flux boundary,10-W should be used to get approximate 98% boundary.However, it may be not easy to separate traces with 10-W distance,Figure 15 is 5-W (W=12 mils)

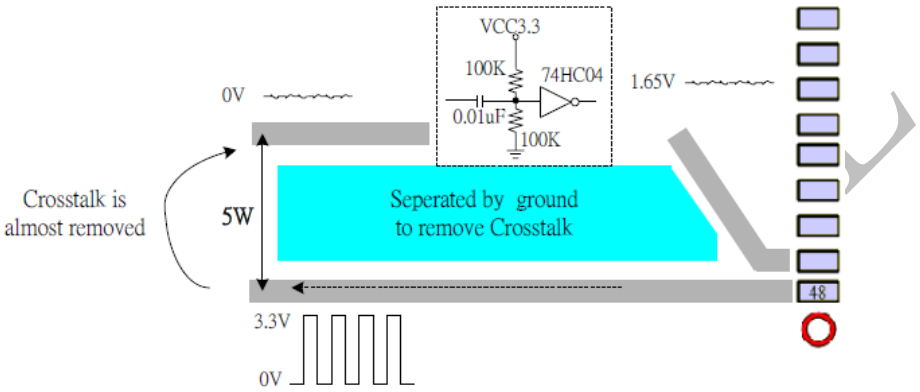

Figure.15 suggested layout

Return Current and Loop Areas

Image Planes.Return path or image planes provide low impedance, shortest possible path for return signal currents. The best image plane is the ground plane for the C-Media USB board.

Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (DP, DM). Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane.

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source – the return current. With DC, the return current takes the way back with the lowest resistance. With a higher frequency, the return current flows along the lowest impedance. This is directly beside the signal.

If this return path, mostly the ground plane, has a slot, the return current has to take another way and the results in a loop area. The larger the area, the more radiation and EMI problems occur. The designer has to make sure that the return current can flow directly underneath the signal trace. Another is to route the signal the same way as the return current flows. The best solution is to avoid any slots in the d reference plane.

ESD Protection System Design Consideration

ESD protection system design consideration is covered of the CM6212+CM9881 PCB. The following are additional considerations for ESD protection in a system.

· Metallic shielding for both ESD and EMI

· Chassis GND isolation from the board GND

· Air gap designed on board to absorb ESD energy

· Clamping diodes to absorb ESD energy

· Capacitors to divert ESD energy

· The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

Anti-pop noise mute circuit

We recommended two kind of the anti pop mute solution here.

• The relay circuit can effectively avoid the pop noise and THD+N can also keep the original audio quality.

• The advantage of MOS circuit is low cost but it may effect the quality of THD+N.

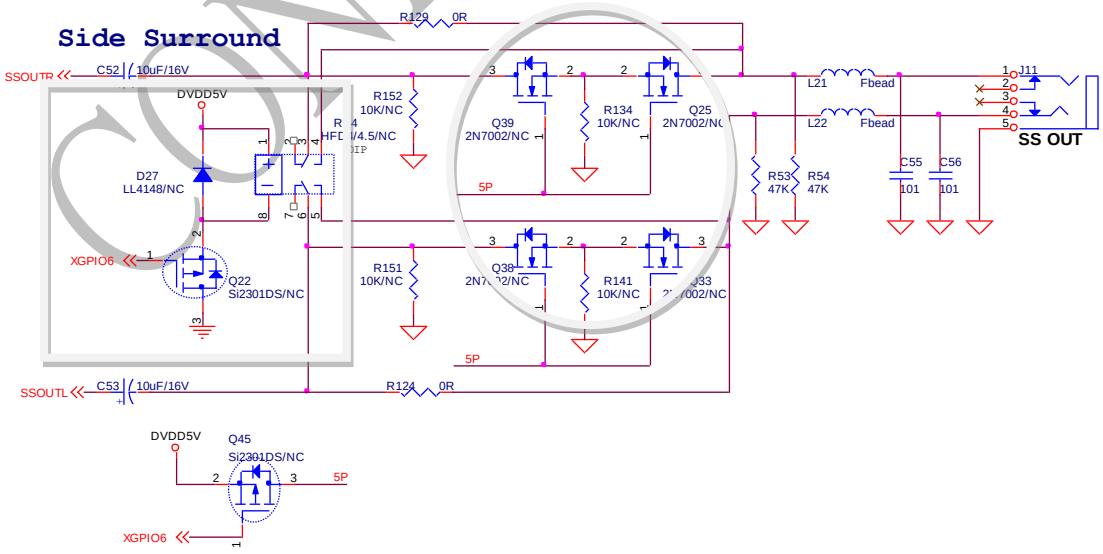

Fig.16 Anti-pop mute circuit